

DERWENT-ACC-NO: 2000-606992

DERWENT-WEEK: 200232

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TITLE: Semiconductor device manufacturing
method involves forming contact hole in insulation
film laminated over element isolation area and transistor
formation area

INVENTOR: MATSUMOTO, K

PATENT-ASSIGNEE: SONY CORP[SONY]

PRIORITY-DATA: 1999JP-0042769 (February 22, 1999)

PATENT-FAMILY:

| PUB-NO | PUB-DATE | |
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| LANGUAGE | PAGES | MAIN-IPC |
| JP 2000243967 A | 007 | September 8, 2000 |
| | H01L 029/786 | N/A |
| US 6372562 B1 | 000 | April 16, 2002 |
| | H01L 021/00 | N/A |

APPLICATION-DATA:

| PUB-NO | APPL-DESCRIPTOR | APPL-NO |
|----------------|-------------------|---------|
| APPL-DATE | | |
| JP2000243967A | N/A | |
| 1999JP-0042769 | February 22, 1999 | |
| US 6372562B1 | N/A | |
| 2000US-0506797 | February 18, 2000 | |

INT-CL (IPC): H01L021/00, H01L021/336, H01L021/762,
H01L021/84,
H01L027/12, H01L029/786

ABSTRACTED-PUB-NO: JP2000243967A

BASIC-ABSTRACT:

NOVELTY - A gate electrode (7) is formed on silicon layer (3) laminated on silicon substrate (1). Source-drain area (8) is formed on layer (3). Impurities are introduced into opening formed in element isolation area (4), and layer (3) to form an impurity diffusion area (11) on an insulating film (2). Insulation film (9) is formed on area (4) and transistor formation area. A contact hole (10) is formed in film (9).

DETAILED DESCRIPTION - The silicon layer is laminated on the substrates via the insulating film (2). The contact hole connects the insulating film (9) to source-drain area, gate electrode and impurity diffusion area.

USE - For manufacturing MOSFET.

ADVANTAGE - Reduces manufacturing cost of semiconductor device.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional views of semiconductor device and manufacturing process of semiconductor device.

Silicon substrate 1

Insulating films 2,9

Silicon layer 3

Element isolation area 4

Gate electrode 7

Source-drain area 8

Contact hole 10

Impurity diffusion area 11

ABSTRACTED-PUB-NO: US 6372562B

EQUIVALENT-ABSTRACTS:

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